A Novel Approach to Digital Gate Design

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Abstract – **Designing the digital gates and circuits has been based on separating the designing levels: circuit level designing and device level designing. In this paper, we will discuss the point that the concept of contact in this distinction is a key-concept and that, by the progress of technology and advancing towards very tiny quantum devices as SET, necessity of having contact, because of its size is considered a basic obstacle; therefore, separating the design into designing the circuit level and device level should be stopped. In this paper, a method of a three level designing has been presented which is based on composing of some parts of the two former designing levels and the new ideas called "contact-less quantum device" and "macro-gate". When the concept of "contact" is omitted, the concept of current in the wires and voltage of the nodes and according to them the KVL and KCL laws should also be omitted. The proper concepts and formulation to be used instead of the omitted ones have been introduced in this paper. In the new designing method, not only the physical dimensions became smaller, but also the new abilities to use the electron phase -which was destroyed before because of contacts- are produced.**

Keywords: **Digital Gate, Contact, Macro-gate, KVL, KCL, Resonant tunneling diode.**

I. Introduction and the basic idea

In the direction of progress of technology and passing MOSFET, several quantum devices have been introduced recently. Some of the most important ones of these devices are the devices based on resonant tunneling such as RTD [1, 2] single-electron devices such as SET [3, 4] the devices based on organic materials such as OFET [5] and the devices based on carbon Nano-tube, for ex. CNFET [6]. These devices have been introduced so as to overcome the limitation of the dimensions of MOSFET, or its uses of energy which cause the limitation of more gate in integrated circuits, but these new devices some of which are even equal to a molecule or few atoms, in size, again- such as the old ones- all of them have one or several contacts because in order to conform with the concepts and meanings which have overcome the minds of the designers for many years, there is no other solution, and these devices must be joined to each other by some wires and these wires must be connected to contacts, and this method has been used so far and the devices and electronic circuits and logic gates have been constructed using this method, but now, we must consider this fact that the contacts and connecting-wires are so thick and in fact, in most of the cases, they are much bigger than the main device. For instance, in a SET, the island and the active parts have the dimensions equal to several nanometers, but the contacts and the wires are the least about 0.1 um; and therefore, they are ten times bigger than the main parts. This condition is also true about RTD and other quantum devices. These contacts are not only big, but also, in many cases, they are the main reason for reducing the speed of quantum devices; for example, in the case of "SET" they have caused the speed of this device to be reduced to nanosecond, while the inherent speed of the device is in order of Pico-second. This is because of the *IDS* current in SET is flowing only from one electron; therefore, it is very small, and a lot of time is needed unit the contacts and connecting wires which have high capacitance because of being bulky are charged or de-charged with this low current. Recently, some circuits have been suggested to make up this velocity reduction, which by coupling the SET by a MOSFET more output current can be produced [7] but it is clear that these suggestions are break of promise because our aim of using SET has been the reduction of dimensions and decreasing the consumption.

By these discussions, we arrive at a point which is the main idea of this paper and it is this point that using the quantum devices together with keeping their contacts is not desirable. We will introduce a three-level segregation called the level of contact-less quantum device, CLQ, and the macro-gate level and the usual circuit-level, and in CLQ we will omit the contact, and in connection with it the connecting wires which joined these devices. We will discuss that these suggestions, in conditions of the progress of technology and production of Nano-metric devices, are necessary actions by which we can answer the existing demands about having many more gates on a single chip than the present ones. By omitting contacts and joining the circuit level to the device level in the design of gates, the laws of circuits such as KVL and KCL will also be omitted and we will introduce the new concepts and relations-used instead of the former ones – in this paper. In section II, following this introduction, we will consider the concept of contact more carefully. In section III, we will present a discussion, the title of which is "Ease and limitation" so as to make the place of basic ideas quite clear. In section IV, we will present the details of the new suggested method and the different kinds of CLQs, and finally in section V, we will conclude the discussion.

II. Going over the concept of contact and its different roles

In this section, we will consider "contact" more carefully and also its role in simplifying the procedure of designing logic and analog circuits up to now. This conversation helps us to understand quite well that by omitting "contact", we should reconsider which points and subjects. In the following part by referring to Fig. 1 we put the different duties of

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"contact" in a list. This figure shows the simplified construction of a resonant-tunneling-diode and its energy levels as a sample of semiconductor quantum devices.

A: In Fig. 1, we see the source contact. From this contact, electron is injected into the device *by a thermal distribution* (the term "*i*" in the picture) which is the first role of the contact. (Injecting electron into the device by a thermal distribution, independent of every other thing).

B: Some part of entering electron wave leaves the device and some of it returns to the source contact (term "*r*" in the picture). Absorbing any amount of the wave returning from the device, without producing any change in the device operation, is the second duty of the contact.

C: On the drain side, the electron wave which is going out of the device *having any sort of specifications* (momentum, energy, etc.) is absorbed in the drain contact (the term "*o*" in the picture) without any change in the device characteristics and this is the third role of the contact.

D: Taking a one dimensional integral on the momentum of the electrons going out of the device and making a term called *current*, which is actually the *total current of all the existing electrons* in the device (and as a result the omission of all the quantum aspects and the detailed distribution of the individual electrons in different momentums and not paying attention to other parameters such as energy and so on), is the fourth role of the contact (the term "I_{DS}" in the picture). Note that all the four above mentioned roles have a firm relation with the size of the contact that should be big enough if it should carry out those roles.

Hear after we call these kinds of contacts, which have a direct contribution on the current, the *first type contact*. Another sort of contacts, which we call them the *second type contact* will be introduced later.

Now if we, once more, look at this issue bearing in mind the progress of technology and using of tiny quantum devices in designing the logic gates, we see that the (first type of) contacts have been useful exactly for the reason of being bad. They have been permitting the design, to be divided into the binary levels, i.e. the level of the device design and the level of the circuit design, but only when they are large and big. And if we notice this result carefully, we completely see that we have no other choice except accepting this conclusion, and in future, the contact, and in connection with it, the separation of the circuit-device, and any other thing related to them, must be omitted from the design of the gate, and this is the basic idea of this paper, and it will be explained more clearly in our next discussions.

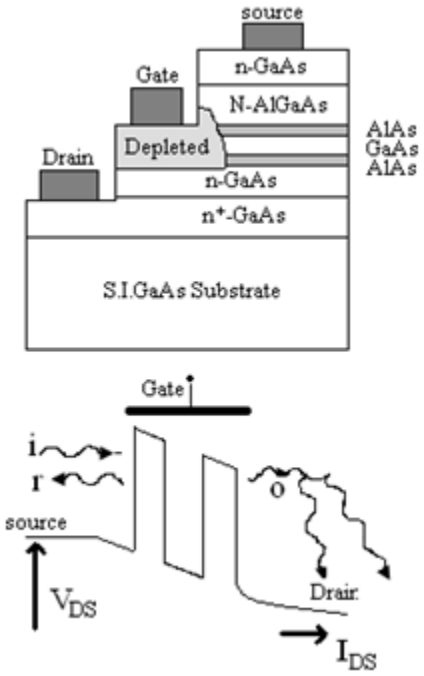

Figure 1. A sample quantum device with type one (source and drain) and type two (gate) cantacts. Input (i term), output (o term), and reflecte waves (r term) are also shown on the figure as well as current (Ids term) and voltage (Vds term)

III. The ease and limitation

By omitting the concept of "contact" which is the point of distinction and separation of the design into the designing levels of device and circuit, because it produces sufficiency of *current* in describing a device responses, these two designing levels are necessarily joined to each other, and in fact, the whole problem is reduced to a problem in designing at the device level, and the problem of designing at the circuit level is canceled. This issue isn't desirable because the above mentioned distinction had many privileges, and we can say that a main part of progresses obtained in the recent decades was because of this distinction. In fact, this distinction is set and accepted so well that the electronic experts have been divided into two groups: the experts in circuits and the experts in devices, and these two groups have nearly a good cooperation and have nearly no problem with each other. The contact of these two groups is actually the concept of the *circuit-model of the device* which is produced with the help of physical investigations done by the experts in the field of device in such a way that it includes all physical results, but makes them accessible in the form of a circuit which lacks any kind of physical variable (such as the profile of electric field, the profile of the density of carriers, and so on.) different from the voltage and the current, and therefore, it is realized and used easily by the experts in the field of circuit, and it could be said that whatever logic gates and analog-integrated circuits have been suggested up to now, have been the results of this valuable and interesting segregation. But on the other hand we observed that this segregation depends strongly on the concept of contact, and the contact should also have big dimensions so as to be

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possible for us to do this segregation, and it is at this point that the basic barrier which exists in the way of progress and using the quantum devices effectively, shows its existence. To continue the progress in this field doesn't mean that we can forget about the segregation completely and by omitting the concept of contact, reduce the whole thing to designing at the device level, but while we also keep some of segregation, we should try to use something else.

Without introducing a new limitation, the whole story as it was told before, is reduced to designing at the device level, and this design which should replace both of the former design levels in this way, it means the single-piece design of the gate at the device level (without contact and as a result, without any usage of the concept of the circuit) will be extremely difficult. As a conclusion, we can say that:

A: Single-piece designing the gate (and any kind of analog circuit as well) without any kind of limitation, is a very difficult job.

B: Using the contact and following it the concepts of KCL and KVL and the circuit model, all of which have been of an *optional limitation* in designing the gate which have made the designing work very easy by separating designing into two designs of the device-design and the circuit-design.

C: In present conditions, the limitation of using contact is a barrier on the way of designing the gate.

D: An optional and new limitation should be introduced which doesn't require the big physical dimensions, and at the same time, has a very effective application in simplifying the design.

Continuing the discussion, the limitation required, and following it, we will introduce the required segregation and the connecting rules of the sides of segregation.

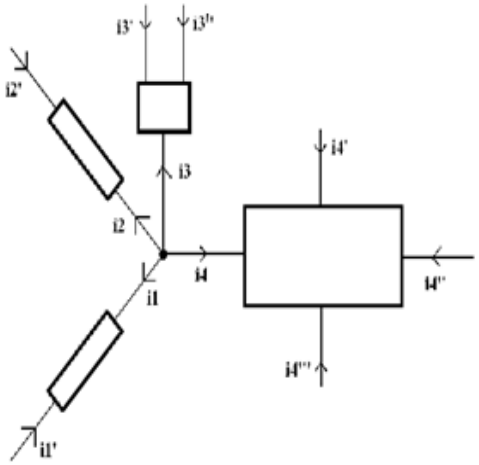

Fig. 2: KCL and its two statements.
Statement a) Sum of all outgoing currents from a node is equal to zero
i1 + i2 + i3 +i4 = 0

Statement b) Sum of all outgoing currents from a circuit element is equal to zero
i1 + i1' = 0 i2 + i2' = 0 i3 + i3' + i3'' = 0 i4 + i4' + i4'' + i4''' = 0

The first statement is always true but the second statement is only true when the circuit elements be in far distance from each other

IV. The details of the new method

The new idea which is being introduced is mainly of some application in designing the gates which are going to be made on a semiconducting material with high mobility such as silicon or GaAs and for other cases such as molecular electronics which are made with organic material of low mobility, similar ideas can be presented. Figure 3 shows a picture from a typical gate designed by using the new method. The first point is that we suggest an elementary division for designing the "gate" which has two design-levels as before:

The level of contactless-quantum-device.

The level of the macro-gate.

In the following paragraphs, we will explain the two mentioned designing levels, and also, the way of their connection with each other in more details:

A. Macro-Gate

Macro-gate (or macro-circuit or macro-device), from outside view, is something that has usual contacts; therefore, the macro-gates are joined to each other by wires such as the devices in the ordinary circuits so as to make the bigger circuits, and KVL and KCL rules come true about them. But as we will see the point with more details, their inputting contacts are of second type of contact that don't carry any current, and also the voltage of their outputting contacts are fixed on the basis of an optional limitation (Fig. 5). In these conditions the mathematical relationship -explaining their behavior- can be written as the following equations:

$$i_k = f_k(v_1, v_2, v_3, ...v_{m-1}, v_m) \quad (1)$$
$$k = 1,2,3,.....,n-1,n$$

Here, according to Fig. 5, it has been supposed that our macro-gate contains *n* number of output contacts and *m* number of input contacts. This formula has been obtained from the general formula (written below) for the devices which has *m+n+1* number of contacts, in this way that the voltage of outputting contacts (because of being fixed) and the current of the inputting contacts (because they are of the second type) has been put aside.

$$i_k = f_k(v_1, v_2, v_3, ...v_{m+n-1}, v_{m+n}) \quad (2)$$
$$k = 1,2,3,.....,m+n-1,m+n$$

We have called these devices, macro-gate, because we expect them to do more work than the work of a simple gate, for example they might have held (in them) a several-bit full adder. Considering the analog applications, they can also be called macro-circuits because, for example, they could perform the job of an op-amp. Even if, we call them macro-device, it will be because of this point that they are placed in the limits of the laws of circuit, considering them from outside. As a device has also this quality that it is described from outside with I/V relations, but at the same time they are much more expanded than a usual device (for example, a FET transistor). But since this paper has been written according to digital aspect, we will call them macro-gate in this paper. Macro-gate has a basic limitation that all of its dimensions should be smaller than the

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electron's coherence length. This limitation has an important role which will be discussed later. From inside view, a macro-gate as is shown in Fig. 3, consists of some contactless quantum devices.

B. The quantum device

The basic optional limitation which has been used for this device is that only the electron with specific energy should exist in the device. According to Fig. 3, by using an element of RTD on the fading line, this limitation is used. In this condition, RTD is acting like a filter which only lets the electrons -having a fixed amount of energy- to pass through it. This action in addition to the limitation which was described before: that the amount of supply voltage is fixed and small, causes the electron has nearly fixed amount of energy in the whole of the macro-gate. This condition, in addition to the point that the dimensions of macro-gate have been considered smaller than the coherent length, causes the ballistic transport of electrons with fixed amount of energy in all of the quantum devices existing inside a macro-gate. The intermediate quantum devices as we see them in Fig. 3, don't have contacts and they are connected to each other directly. Of course, the last quantum devices have been connected to macro-gate contacts, and any amount of outgoing waves existing in these devices are delivered to contacts.

Different kind of quantum devices acting in these conditions and the physical relationships describing their behaviors can be listed in the following way:

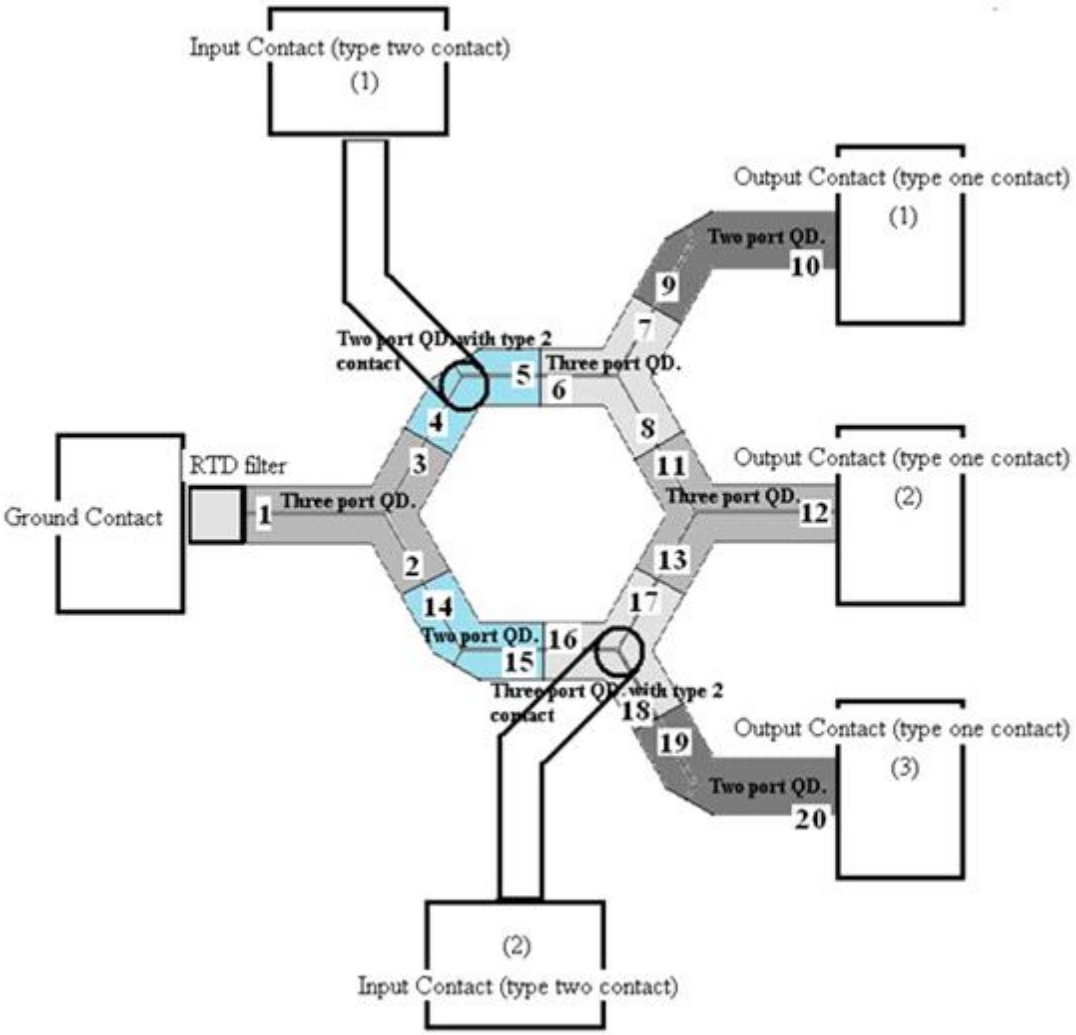

Figure 3. A schematic diagram of a Macrogate that has two inputs, 3 outputs and a ground contact and consists of 8 different quantum devices (QDs) plus a RTD filter. As shown all internal nodes, input contanct and output contants are numbered to make ready system of equations of the Macrogate (see text)

B.1. The two-port device:

In a two-port device, as we see in Fig. 4, we have two entering waves and two outgoing waves, and the descriptive formulas of the device can be written as

$$\begin{vmatrix} O1 \\ O2 \end{vmatrix} = \begin{vmatrix} r & -t^* \\ t & -r^* \end{vmatrix} \begin{vmatrix} i1 \\ i2 \end{vmatrix} \qquad (3)$$

r and t are the coefficients of reflection and transmission,

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and we have $r^2 + t^2 = 1$. They are functions of physical structure of the device. The two-port device, as in figure 3, can have a contact of the second type, and in this situation, the coefficients of transmission and reflection are not a fixed and permanent value, but they are a function of the voltage of this contact. An example of the two-port quantum device which doesn't have the second type of contact is the resonant tunnel diode, and an example of a two-port quantum device having the second type of contact, is the resonant tunnel-transistor. Of course, these devices, when have been made before, they have had the contacts on their two ends but, here they are of very small dimensions and don't have any contacts on their two ends.

B.2. The three-port device:

In the three-port device, as we see in the Fig. 4, there are three entering waves and three outgoing waves which every one of the outgoing waves include three parts. The descriptive relationship of this device, in general conditions is in the following form:.

$$\begin{vmatrix} O1 \\ O2 \\ O3 \end{vmatrix} = \begin{vmatrix} t_{11} & t_{12} & t_{13} \\ -t_{12}^{*} & t_{22} & t_{23} \\ -t_{13}^{*} & -t_{23}^{*} & t_{33} \end{vmatrix} \begin{vmatrix} i1 \\ i2 \\ i3 \end{vmatrix} \qquad (4)$$

This device totally has 6 parameters which may be fixed (they may be determined while the device is being constructed) and it is also possible that the device has a contact of the second type (look at Fig. 3) which in this case, these parameters will be a function of the voltage of this contact. This device can be used as the "electron-wave distributor" and also "electron-wave adder" which may has an input (i.e. control) contact.

B.3. The four-port device and other kinds:

The four-port devices and other form having more ports are the extensions of the former devices and are described according to similar formulas, but we exact that, in the same way in the present designing method, the devices are usually of three-wire or two-wire connections, and the devices with more more wire-connections are not usually used, in this new design, because of keeping away of high degree of complexity, the two-port and three-port devices should only be used.

C. The laws of connecting the quantum devices -the calculation at the macro-gate level

In designing method based on the separation of circuit/ device, the calculations of the circuit level were done according to the aim of finding the currents and voltages at the circuit outputs of interest. These calculations were based on KVL and KCL and I/V relations of the devices. The sentences similar to the sentences mentioned above for the new method are mentioned below.

The aim of the calculations of the macro-gate-level is finding the current at the outputs of the macro-gate (the Equ. 1). This calculation is done by knowing the O/I relationship of quantum devices (the Equs. 3 & 4) in one way and the following formula in the other way:

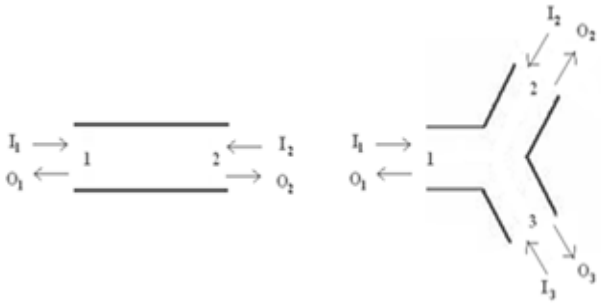

Figure 4. A two port (at left) and a three port (at right) quantum device with indexed input and output waves

$$\begin{cases} I_m = O_n \\ I_n = O_m \end{cases} \quad \text{if m \& n are connected internally}$$
$$I_n = 0 \quad \text{if n is an ending node}$$
$$I_n = 1 \quad \text{if n is a begining node} \qquad (5)$$
$$I_n = -O_n \quad \text{if n is an internal closed end node}$$

Here, it has been assumed according to Fig.3 that all the ports of quantum devices have been numbered. *In* is the amplitude of the entering wave toward the port *n*th. and *On*, is the amplitude of outgoing wave from the port *n*th. Moreover, as the picture shows every port of a quantum device can be connected to a port of another device or to the output of the entering RTD or to an output contact or it can be left open (the connection of several ports is not permitted) which, the relationship of interest in every case, has been presented in the formula mentioned above. By solving the equations mentioned above together with equations describing the quantum devices forming the macro-gate in a system of equations as it was being done in the method of solving a usual circuit, the amounts of entering and outgoing waves are calculated and then, the currents of macro-gate-contacts can be calculated in the following way:

$$i_l = \frac{-q\hbar k}{m^*} |I_l|^2 \qquad (6)$$

In this formula, I_l is amplitude of entering wave into the contact *l*th. and i_l is the current of the contact *l*th. q is the electron charge, m^* is its effective mass and k is its wave vector.

V. Conclusion

In this paper, it was first discussed that using the quantum devices in the way that now, every one of them has several contacts, is not useful, and it is a barrier in the way of progress in minimizing the size of gates. Then, we discussed the fundamental connection existing between having contacts and the device-circuit distinction, and the connection of this distinction with KVL and LCL was made clear. Then a concept was presented according to which, we can say that limitation and ease are two different aspects which are related to each other and this concept that selecting the limitation in consideration, and the ease which is produced by this limitation, is a free choice and it can be selected in such a way that it doesn't require the big physical dimension was

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emphasized. Then, a method of designing based on new limitations was suggested, and its details were discussed and then the substitutions of KVL and KCL were presented. This designing method which is a three-level designing method, instead of the two-level designing method, is as follows:

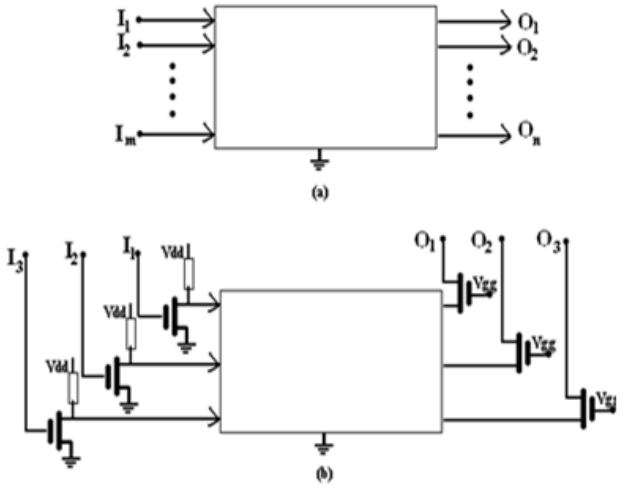

Figure 5. (a) Schematic circuit diagram of a Macrogate with m inputs and n outputs
(b) An example of using Macrogate in a circuit. Output FETs buffer the output contacts of Macrogate and keep them in a constant voltage

1. The first designing level: This designing level is similar to the circuit level design which was used to be done in the past: In this design, the macro-gates and the other electronic devices, all of which have contacts, are joined to each other by usual wires and connections. The macro-gates by their introducing formulas (such as Equ. 1) and other electronic devices with their I/V relationships are introduced to this level, and their connection rules are KVL and KCL. In the case of macro-gates, this necessity exists that the voltage of their output contacts should be fixed.

2. The second designing level or the macro-gate designing level: In this level, the quantum devices are connected to each other so as to build up a macro-gate. The quantum devices lack contacts and with their wave-relations (such as the Equs. 3 & 4) are introduced to this level. The connecting rules of these devices to each other are the Equs. 5 & 6. This necessity exists that the whole size of macro-gate must be smaller than the coherence length of electron and a filtering RTD should exists on the fading line as shown in figure 3.

3. The third designing level or the designing level of quantum-devices. This level is the same as the designing level of the device, in the past, and in this level, the two-port or three-port quantum devices, with or without second type of contacts, are designed and this necessity exists that, they don't have the first type of contacts. The fundamental equations are the same physics-equations such as Schrödinger and Poisson equations and the results are described and explained in the form of Equs. such as the Equs. 3 and 4 and then, they are introduced to the upper levels as mentioned. Continuing the discussion, we will discuss some complementary points.

- The reader of this paper probably feels that there is a connection between this discussion and the subject of quantum computers. In fact, this relation exists because as it was mentioned before, all through the inner devices of a macro-gate, the electron-phase is preserved, and we can construct a macro-gate that can perform the quantum calculations. We will leave the detailed of this point to the next works.

- In fact, some of the electron-wave inside the macro-gate, in addition to the basic made is also scattered into a series of secondary modes which if the accurate calculations of the currents are of our consideration, these scattered waves should be considered. This subject, in present application which was the main emphasis on digital applications, is not of much importance, but in the analogue applications that the currents must be calculated precisely, it is of importance. The detailed description of this subject will also be leaved to the later works.

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